#8A Amdt
M. Braunson
10/14/02

Our Reference: ESI-116-A PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Patrick F. Leonard
Serial No.	09/680,342
Filing Date:	October 5, 2000
Examiner/Art Unit	C. Kao
Title:	METHOD AND APPARATUS FOR EVALUATING INTEGRATED CIRCUIT PACKAGES HAVING THREE DIMENSIONAL FEATURES

AMENDMENT

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

The Office Action dated April 26, 2002 has been received and carefully reviewed. Please amend the above-identified patent application as indicated below.

In the specification:

Replace the paragraph on page 1, lines 4 through 6 with the following paragraph:

A1

Under the provisions of 35 U.S.C. 119(e) and Patent Rule 55, Applicant claims the benefit of the following prior provisional application, Application No. 60/157,763 filed October 5, 1999.

Replace the paragraph on page 1, beginning on line 23 through page 2, line 2 with the following paragraph:

A2

The substrate or wafer to which the QFP or BGA attaches includes a corresponding array of pads to which the wires ("leads") of the QFP or balls of the BGA